WHAT IS CLAIMED IS:

1. A loop circuit for producing an internal clock signal that tracks a received reference clock signal comprising:

a phase comparator for comparing a feedback signal derived from said internal clock signal with said reference clock signal;

a setting counter that is adjusted by said phase comparator after a particular net number of either lead or lag comparisons by said phase comparator; and

a compensation component for receiving said reference clock signal and, based on said setting counter, producing said internal clock signal.

2. The loop circuit of claim 1 wherein said feedback signal is substantially the same signal as said internal clock signal.

3. The loop circuit of claim 1 wherein said feedback signal is a delayed version of said internal clock signal.

4. The loop circuit of claim 1 wherein said reference clock signal is a clock signal from circuitry external to said loop circuit.

5. The loop circuit of claim 1 wherein said reference clock signal is received from an oscillator.

6. The loop circuit of claim 1 wherein said phase comparator comprises:

a phase detector for producing lead or lag output signals indicative of a measured phase difference

between said feedback signal and said reference clock signal.

7. The loop circuit of claim 6 wherein said phase comparator further comprises:

a low-pass noise filter for receiving said lead or lag output signals from said phase detector, said low-pass noise filter adjusting said setting counter after said particular net number of either lead or lag comparisons by said phase detector.

8. The loop circuit of claim 7 wherein said low-pass noise filter comprises:

an up down counter that is set to an initial value, said up down counter that is incremented or decremented based on said lead or lag output signals from said phase detector; and

a programmable logic circuit that adjusts said setting counter once said up down counter reaches an upper or lower threshold value.

9. The loop circuit of claim 8 wherein said low-pass noise filter has a programmable bandwidth, at least one of said upper and lower threshold values of said programmable logic circuit being controlled by a bandwidth control signal.

10. The loop circuit of claim 9 wherein said bandwidth control signal is provided directly by user inputs.

11. The loop circuit of claim 9 wherein said bandwidth control signal is provided by RAM bits from a programmable logic device.

12. The loop circuit of claim 9 wherein said bandwidth control signal is adjustable during operation of said loop circuit.

13. The loop circuit of claim 8 wherein said up down counter is reset to said initial value once said setting counter has been adjusted.

14. The loop circuit of claim 8 wherein said setting counter is not reset once said setting counter has been adjusted.

15. The loop circuit of claim 8 wherein said setting counter is reset to a value other than said initial value once said setting counter has been adjusted.

16. The loop circuit of claim 8 wherein said up down counter is reset to said initial value once said up down counter reaches its maximum or minimum counter value.

17. The loop circuit of claim 8 wherein said up down counter is reset to said initial value once said up down counter reaches a reset level.

18. The loop circuit of claim 17 wherein said reset level is adjustable during operation of said loop circuit.

19. The loop circuit of claim 1 wherein:

said loop circuit is a delay-locked loop circuit; and

said compensation component comprises a controlled delay line for producing said internal clock signal.

20. The loop circuit of claim 1 wherein:

said loop circuit is a phase-locked loop circuit; and

said compensation component comprises a controlled oscillator for producing said internal clock signal.

21. A programmable logic device comprising the loop circuit of claim 1.

22. The programmable logic device of claim 21 further comprising:

a plurality of regions that utilize said input clock signal; and

clock signal distribution circuitry for distributing said internal clock signal to said regions.

23. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic device as defined in claim 21 coupled to the processing circuitry and the memory.

24. A printed circuit board on which is mounted a programmable logic device as defined in claim 21.

25. The printed circuit board defined in claim 24 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the programmable logic device.

26. The printed circuit board defined in claim 25 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

27. An integrated circuit device comprising the loop circuit of claim 1.

28. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

an integrated circuit device as defined in claim 27 coupled to the processing circuitry and the memory.

29. A printed circuit board on which is mounted an integrated circuit device as defined in claim 27.

30. The printed circuit board defined in claim 29 further comprising:

memory circuitry mounted on the printed circuit board and coupled to the integrated circuit device.

31. The printed circuit board defined in claim 30 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the memory circuitry.

32. A loop circuit for producing an internal clock signal that tracks a received reference clock signal comprising:

a phase comparator for comparing a feedback signal derived from said internal clock signal with said reference clock signal;

a compensation component for producing said internal clock signal based on said reference clock signal by adjusting said internal clock signal after a particular net number of either lead or lag comparisons by said phase comparator, wherein said particular net number is controlled by a bandwidth control signal.

33. The loop circuit of claim 32 wherein said bandwidth control signal is provided directly by user inputs.

34. The loop circuit of claim 32 wherein said bandwidth control signal is provided by RAM bits from a programmable logic device.

35. The loop circuit of claim 32 wherein said bandwidth control signal is adjustable during operation of said loop circuit.

36. A method of producing an internal clock signal that tracks a received reference clock signal comprising:

comparing the phase of a feedback signal derived from said internal clock signal with the phase of said reference clock signal;

counting the number of lead or lag comparisons made between the phase of said internal clock signal and the phase of said reference clock signal; and

using a compensation component for producing said internal clock signal based on said feedback signal, said compensation component adjusting said internal clock signal after a particular net number of either lead or lag comparisons has been counted.

37. The method of claim 36 wherein said particular net number is controlled by a bandwidth control signal.

38. The method of claim 37 wherein said bandwidth control signal is provided directly by user inputs.

39. The method of claim 37 wherein said bandwidth control signal is provided by RAM bits from a programmable logic device.

40. The method of claim 37 wherein said bandwidth control signal is adjustable during said production of said internal clock signal by said compensation component.